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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/731,298	12/09/2003	Wagdi W. Abadeer	END920030103US1	3646

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EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 01/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/731,298	ABADEER ET AL.	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/09/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 8 and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Morishita et al. (USP 5757175).

Morishita et al. discloses in figure 7 a circuit, and a method thereof, comprising a current mirror (2, NT2) coupled to a tunneling leakage monitor (PT3, PT4 and circuit CVC in figure 6), the tunneling leakage monitor including a tunneling leakage monitoring device (in the CVC), the current mirror adapted to force a tunneling leakage current of the tunneling leakage device to a predetermined current value; and a voltage buffer (CMP and DT in figure 6) coupled to the leakage monitor, the voltage buffer adapted to generate an output voltage (INVCC) based on a voltage level developed across the leakage monitoring device when the tunneling leakage current is at the predetermined current value.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2-4, 13 and 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morishita et al. (USP 5757175) in view of Maneatis (USP 6462527).

As to claims 2, and 16, Morishita et al.'s figures 6 and 7 show all limitations of the claim except for the current mirror includes an adjustable current source and means to adjust a current generated by the current source. However, Maneatis's figure 3 a current mirror including an adjustable current source (Reference System). Therefore, it would have been obvious to one having ordinary skill in the art to use Maneatis's figure 3 for Morishita et al.'s current mirror for the purpose of having more flexibility for selecting and generating various currents to the CVC circuit in order to generate various reference voltages.

As to claim 3, the modified Morishita et al.'s reference further fail to show that the current source is a band gap current source. However, it is notoriously well known in the art that bandgap current source generates current independent of temperature, thereby provides accurate desired current. Therefore, it would have been obvious to one having ordinary skill in the art to use bandgap current source to provide current to the current mirror circuit for the purpose of improving the performance of the circuit.

As to claims 4 and 17, the modified Morishita et al.'s reference shows that the means (the switches and the switch selection circuit, not shown, in Maniatis's figure 3) to adjust a current generated by the current source is a digital to analog converter.

As to claim 13, the output voltage of the reference voltage (supply voltage) is varies depending on the number of switches that are closed. The value of the reference voltage with only one closed switch is seen as a nominal value. Thus, the voltage level of the on-chip power supply for the best case process integrated circuit is lowered when no switch is closed; and the

voltage level of the on-chip power supply for the worst case process integrated circuit is raised when more than one switches are closed.

5. Claims 5, 10, 12 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morishita et al. (USP 5757175) in view of Maniatis (USP 6462527) and Shyr et al. (USP 6472897).

As to claims 5 and 10, the modified Morishita et al.'s reference shows all limitations of the claim except for fuse circuit controls the DAC. However, Shyr et al.'s figure 1 shows fuse circuit 14 controls the DAC. The benefit of using the fuse circuit is the output control signal irreversible when fuse is blown. Therefore, it would have been obvious to one having ordinary skill in the art to use fuse circuit to control the DAC in the modified Morishita et al.'s reference for the purpose of permanently closing or opening the switches in the DAC.

As to claim 12, it is seen as an obvious design preference to select the current of known value is to be about equal to the tunneling leakage current of a worst-case process integrated circuit chip dependent upon particular environment of use to ensure optimum performance.

6. Claims 11 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morishita et al. (USP 5757175).

As to claim 11, Morishita et al.'s figures 6 and 7 show all limitations of the claim except for the step of performing a burn-in test of the integrated circuit chip while forcing the current of known value through a tunneling current leakage monitor device. However, it is notoriously well known in the art that burn-in test is for ensuring the circuit operates properly in a high voltage condition. Therefore, it would have been obvious to one having ordinary skill in the art to performing a burn-in test of the integrated circuit chip while forcing the current of known

value through a tunneling current leakage monitor device for the purpose of ensuring the circuit operates properly in a high voltage condition.

As to claim 14, it is inherent that the first value current in a burn-in operation of the integrated circuit is higher than a second current value in a normal operation because the supply voltage in a burn-in operation is higher than the supply voltage in a normal operation.

7. Claims 6 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morishita et al. (USP 5757175) in view of Stubbs et al. (USP 6597619).

Morishita et al.'s figures 6 and 7 show all limitations of the claim except for a voltage regulator coupled to the voltage buffer. However, Stubbs et al.'s figure 3 shows a voltage regulator (250) coupled to the buffer circuit (200) in order to reduce noise. Therefore, it would have been obvious to one having ordinary skill in the art to add a voltage regulator to the output of Morishita et al.'s buffer for the purpose of reducing noise.

8. Claims 7, 9 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morishita et al. (USP 5757175) in view of Ngo et al. (USP 5942934).

Morishita et al.'s figures 6 and 7 show all limitations of the claim except for that the leakage monitor device is a gate capacitor. However, Ngo et al.'s figure 2 shows a voltage generating circuit having a capacitor (C1) coupled to the input of the buffer circuit (OA1) in order to filtering noise at the input of the buffer circuit. It is also well known in the art that gate capacitor is more compact than regular capacitor. Therefore, it would have been obvious to one having ordinary skill in the art to add a gate capacitor coupled to the input of Morishita et al.'s buffer circuit for the purpose of filtering noise. Thus, the newly added capacitor is a part of the leakage monitor device.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references are cited as interest because they show some circuits analogous to the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Quan Tra
Patent Examiner

January 12, 2005